## AMENDMENTS TO THE CLAIMS

1. (currently amended) An arithmetic circuit comprising:

a plurality of registers;

an arithmetic unit, for regarding, as inputs, values entered in said multiple registers; and

a plurality of memories, wherein reading of multiple variables from said plurality of memories to said plurality of registers is performed during the same reading cycle by way of a pipeline process performed by said arithmetic unit said arithmetic unit being a multiplier adder for, based on values $x_1$, $x_2$, $x_3$ and $x_4$ having an r-bit length that are respectively input to a first register, second register, third register and fourth register, providing, in a single operational cycle, a result Q for $x_1 + x_2 \cdot x_3 + x_4$ having a length of 2r bits or 2r+1 bits.

2. (canceled)

3. (currently amended) The arithmetic circuit according to claim 12, wherein said multiple memories include a first memory and a second memory; and wherein, at a stage for writing an operation result, which follows the operation stage of said pipeline process, lower r bits $Q_L$ of said operation result Q are recorded in said first memory, and upper bits $Q_H$ of said operation result Q, excluding said bits $Q_L$, are recorded in said fourth register, while at a stage for reading variables from said registers, which follows said writing stage, simultaneously, a variable $x_1$ is read from said first memory and is stored in said first register, and a variable $x_3$ is read from said second memory and is stored in said third register.

2

4. (original) The arithmetic circuit according to claim 3, wherein said first memory and said second memory are two-port memories having one data writing port and one data reading port.

5. (original) The arithmetic circuit according to claim 3, wherein said first memory is a two-port memory having one data writing port and one data reading port, while said second memory is a single-port memory having one port for the writing and reading of data.

6. (currently amended) An arithmetic circuit comprising:
   a plurality of registers;
   an arithmetic unit, for regarding, as inputs, values entered in said multiple registers; and
   a plurality of memories, wherein reading of multiple variables from said plurality of memories to said plurality of registers is performed during the same reading cycle by way of a pipeline process performed by said arithmetic unit. The arithmetic circuit according to claim 1, wherein said arithmetic unit being~~is~~ a multiplier adder for, based on values $x_1$, $x_2$, $x_3$, $x_4$ $x_5$ and $x_6$, having an r-bit length, that are respectively input to a first register, a second register, a third register, a fourth register, a fifth register and a sixth register, and for providing, in a single operational cycle, the operation results Q for $x_1 + x_2 \cdot x_3 + x_4 \cdot x_5 + x_6$, which have a length of 2r bits or 2r+1 bits.

7. (original) The arithmetic circuit according to claim 6, wherein said multiple memories include a first memory, a second memory and a third memory; wherein, at a stage for writing an operation result, which follows the operation stage of said pipeline process, lower r bits $Q_L$ of said operation result Q are recorded in said first memory, and upper bits $Q_H$ of said

3

operation result Q, excluding said bits $Q_L$, are recorded in said sixth register; and wherein, at a stage for reading variables to said registers, which follows said writing stage, simultaneously, a variable $x_1$ is read from said first memory and is stored in said first register, a variable $x_3$ is read from said second memory and is stored in said third register, and a variable $x_5$ is read from said third memory and is stored in said fifth register.

8.  (original) The arithmetic circuit according to claim 7, wherein said first memory is a two-port memory having one data writing port and one data reading port, and said second memory and said third memories are single-port memories having one port for the writing and the reading of data.

9.  (currently amended) An arithmetic method using an arithmetic circuit that includes an arithmetic unit, which has multiple input registers and multiple memories, comprising the steps of:

    performing an arithmetic operation based on values stored in said input registers;

    writing the results of said arithmetic operation in said input registers or said memories; and

    reading multiple variables from said multiple memories and storing said variables in said multiple input registers during the same pipeline stage,

    said arithmetic unit being a multiplier adder for, based on values $x_1$, $x_2$, $x_3$ and $x_4$ having an r-bit length that are respectively input to a first register, a second register, a third register and a fourth register, providing, in a single operational cycle, the operation results Q for $x_1 + x_2 \cdot x_3 + x_4$ having a length of 2r bits or 2r+1 bits.

4

10. (canceled)

11. (currently amended) The arithmetic method according to claim 9̶1̶0̶,
    wherein said multiple memories include a first memory and a second
    memory, further comprising:
        a writing step in a pipeline process of said arithmetic unit for
        recording, in said first memory, lower r bits $Q_L$ of said operation
        result Q, and for recording, in said fourth register, upper bits $Q_H$ of
        said operation result Q, excluding said bits $Q_L$; and
        a reading step of performing, at the same reading stage in said
        pipeline process, the reading of a variable $x_1$ from said first
        memory and storing said variable $x_1$ in said first register, and the
        reading of a variable $x_3$ from said second memory and storing
        said variable $x_3$ in said third register.

12. (original) The arithmetic method according to claim 11, wherein said first
    memory and said second memory are two-port memories having one
    data writing port and one data reading port.

13. (original) The arithmetic method according to claim 11, wherein said first
    memory is a two-port memory having one data writing port and one data
    reading port, while said second memory is a single-port memory having
    one port for the writing and reading of data.

14. (currently amended) An arithmetic method using an arithmetic circuit that
    includes an arithmetic unit, which has multiple input registers and
    multiple memori s, comprising the steps of:
        performing an arithmetic operation based on values stored in said

5

input registers;

writing the results of said arithmetic operation in said input registers or said memories; and

reading multiple variables from said multiple memories and storing said variables in said multiple input registers during the same pipeline stage.

~~The arithmetic method according to claim 9,~~ wherein said arithmetic unit is a multiplier adder for, based on values $x_1$, $x_2$, $x_3$, $x_4$ $x_5$ and $x_6$, having an r-bit length, that are respectively input to a first register, a second register, a third register, a fourth register, a fifth register and a sixth register, and for providing, in a single operational cycle, the operation results Q for $x_1 + x_2 \cdot x_3 + x_4 \cdot x_5 + x_6$, which have a length of 2r bits or 2r+1 bits.

15. (original) The arithmetic method according to claim 14, wherein said multiple memories include a first memory, a second memory and a third memory, further comprising:

a writing step in a pipeline process of said arithmetic unit for recording, in said first memory, lower r bits $Q_L$ of said operation result Q, and for recording, in said sixth register, upper bits $Q_H$ of said operation result Q, excluding said bits $Q_L$; and

a reading step of performing, at the same reading stage of said pipeline process, the reading of a variable $x_1$ from said first memory and storing said variable $x_1$ in said first register, the reading of a variable $x_3$ from said second memory and storing said variable $x_3$ in said third register, and the reading of a variable $x_5$ from said third memory and storing said variable $x_5$ in said fifth register.

6

16. (original) The arithmetic method according to claim 15, wherein said first memory is a two-port memory having one data writing port and one data reading port, while said second and third memories are single-port memories having one port for the writing and reading of data.

7

JP920000304US1                                                      Appl. No. 10/023,147

PAGE 9/15 * RCVD AT 12/16/2003 3:20:38 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-1/3 * DNIS:8729306 * CSID:845 892 6363 * DURATION (mm-ss):03-34